REMARKS

This Amendment addresses the issues outstanding from the final Office Action dated February 4, 2009. Favorable reconsideration is respectfully requested.

By this Amendment, without acceding to the rejection, independent Claim 1 has been amended to recite certain distinctive features of Applicants' invention with greater particularity. Claims 4, 5, 24, and 25 have been amended for clarity. As will be explained below, independent Claim 1 (and its dependents) distinguishes patentably from the collective disclosures of Hiraki, Stewart, and Tanzawa.

As now set forth in Claim 1, the first control circuit (of the memory module) receives a first instruction code, which indicates to transfer data stored in the non-volatile memory to the dynamic random access memory, via the dynamic random access memory interface, and receives a second instruction code, which indicates to transfer data stored in the non-volatile memory to the static random access memory, via the static random access memory interface. Claim 1 also now recites that when data stored in the non-volatile memory is to be outputted to outside the memory module, data stored in the non-volatile memory is transferred to at least one of the dynamic random access memory based on the first instruction code and the static random access memory based on the second instruction code, and then any portion of said data transferred to the dynamic random access memory is

outputted to outside the memory module via the dynamic random access memory interface, and any portion of said data transferred to the static random access memory is outputted to outside the memory module via the static random access memory interface.

It is apparent that Hiraki fails to teach or suggest the foregoing features of Claim 1. Note, for example, that Hiraki's flash memory 11, DRAM 12, and SRAM 13 are connected in parallel via bus 16. As such, even assuming *arguendo* that Hiraki's input and output buffers of the flash memory (11IB/11OB), DRAM (12IB/12OB), and SRAM (13IB/13OB) can properly be construed as meeting the claimed dynamic random access memory interface and the static random access memory interface, respectively, Hiraki still fails to teach or suggest that an instruction code is received by such buffers associated with either the DRAM or the SRAM indicating to transfer data stored in the flash memory to the corresponding DRAM or SRAM.

Stewart and Tanzawa, the secondary references, fail to cure Hiraki's deficiencies noted above.

Additionally, Applicants note that the rejection appears inconsistent in the sense that at one point Hiraki's CPU 10 is equated to the claimed first control circuit that accesses the non-volatile memory, the dynamic random access memory, and the static random access memory, and which is a part of the memory module, and at another time Hiraki's

CPU 10 is equated to the claimed second memory controller, which is outside the memory module.

In view of the foregoing, withdrawal of the rejection is respectfully requested. The dependent claims are allowable at least based on their dependence from Claim 1.

A prompt Notice of Allowance is respectfully requested.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 (XA-10365) any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby requested.

Respectfully submitted,

By: /Patrick L. Miller/

Mitchell W. Shapiro
Reg. No. 31,568

Patrick L. Miller
Reg. No. 57,502

Miles & Stockbridge, P.C.
1751 Pinnacle Drive
Suite 500
McLean, Virginia 22102-3833
(703) 610-8651

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